

Application No.: 09/874173

Docket No.: SMQ-043RCE2

REMARKS

Claims 1-20 were presented for examination. Claims 1-20 stand rejected, of which claim 1, 10 and 19 are independent. The following remarks address all stated grounds for rejection, and Applicants respectfully submit that the presently pending claims, as identified above, are in condition for allowance.

I. Claims Being Rejected Under 35 U.S.C. § 102**A. Rejection of Claims 1-3, 5-8, 10-12, 14-17 and 19**

Claims 1-3, 5-8, 10-12, 14-17 and 19 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,758,112 ("Yeager"). Applicants respectfully traverse this rejection for the following reasons.

Claim 1 is directed to a method for managing a number of physical registers using a first structure, a second structure and a third structure. The first structure holds information identifying available physical registers that are free to be assigned as a destination operand for instructions. A physical register assignment is stored in the second structure noting that a selected physical registers is assigned as a destination operand for the architectural register of a selected instruction. The physical register assignment of the selected physical register is transferred from the second structure to the third structure after retirement of the selected instruction. Information identifying the selected physical register as available is transferred from the third structure to the first structure when the architectural register is assigned as a destination operand for a subsequent instruction. Claim 10 is another method claim reciting similar limitations, and claim 19 is a system claim that parallels claim 1. Thus, the invention in Claims 1, 10 and 19 allow a physical register to be characterized as free as soon as the architectural register assigned to its physical register is assigned to a destination operand for a subsequent instruction.

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Yeager discloses a mechanism for saving and restoring register renaming information to facilitate restoration of primary RAM cells in a single clock cycle when a branch prediction is incorrect. Yeager discloses a free list, a mapping table and an active list. The free list contains a list of available registers. The mapping table renames logical registers identified in an instruction with a physical register location for holding values during instruction execution and also output to the active list the old physical destinations associated with the logical registers. *Yeager, col. 4, lines 3-6; col. 7, lines 50-64.* The active list contains an ordered list of all active instructions and the associated old physical destinations and logical addresses received from the mapping table. *Yeager, col. 6, lines 20-24; col. 7, lines 54-62; col. 15, line 39-43.* Instructions are disclosed to be active when they are decoded and remain active until they graduate. *Yeager col. 12, lines 52-56; col 15, lines 39-43.* Yeager discloses that the old physical destinations from the mapping table remain appended to the active list until the instruction graduates, at which time the old physical destination is returned to the free list. *Yeager, col. 7 lines 61-63.* Yeager further discloses that instructions graduate after they have been completed by a functional unit. *Yeager col. 16, lines 1-5.*

Yeager fails to disclose the step of transferring said physical register assignment of said selected physical register from said second structure to a third structure after retirement of said selected instruction. Yeager discloses the old physical destinations from the mapping table as well as the active instructions append to the active list, where an old physical destination remains until the associated instruction graduates. Yeager further discloses an instruction is active until it graduates, and therefore, the active list can never contain old physical destinations of retired instructions. This is distinguished from the third structure of the present invention, which contains physical register assignments of retired selected instructions that were transferred from a second structure after the selected instruction has retired because the active list of Yeager can only receive physical register assignments for active instructions that have not been retired.

Further, Yeager fails to disclose that when said architectural register is assigned as a destination operand for a subsequent instruction, transferring information identifying said selected physical register as available from said third structure to said first structure. As distinguished from the present invention, Yeager discloses that the old physical destination is moved from the active list to the free list upon graduation of a subsequent instruction, not upon

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an assignment of an architectural register as a destination operand for a subsequent instruction. Hence, the present invention increases the number of free physical registers available in a shorter time period as compared to Yeager, and thus increases processing capacity of an associated micro-processor. More specifically, Yeager teaches that after a physical register (i.e., first physical register) is output from a free list and until it is written with a result from a corresponding instruction (i.e., first instruction), the physical register is "busy". If a subsequent instruction needs the values of this physical register (i.e., first physical register), such an instruction must wait until the register is written. After being written, the register (i.e., first physical register) is "ready", and its value is never changed. When a subsequent instruction (i.e., second instruction) changes the corresponding logical register associated with the first physical register to a second physical register, the result will be written into a new physical register (i.e., second physical register). When this subsequent instruction graduates, the old value is no longer needed, and the old physical register (i.e., first physical register) becomes "free" for re-use. Thus, physical registers have unambiguous values. *See*, Yeager Col. 7 50-63 (Emphasis Added).

As discussed above, Applicants assert Yeager teaches moving old physical destinations to the free list from the active list upon graduation of a subsequent instruction, not upon assignment of an architectural register for a subsequent instruction, which is significantly different in terms of structure, function and operation between Applicants' claimed invention and the invention taught by Yeager. Therefore, Yeager's step of retiring the second instruction as a prerequisite to moving a physical register from the active to the free list teaches away from transferring information identifying a physical register as available from the third structure to the first structure when the architectural register associated with the physical register is assigned as a destination operand for a subsequent instruction.

In light of the arguments set forth above, Applicants submit that the Yeager reference fails to disclose all of the elements of claims 1, 10 and 19. Claims 2-3 and 5-8 depend on claim 1 and therefore incorporate all the patentable features of claim 1. Claims 11-12 and 14-17 depend on 10 and therefore incorporate all the patentable features of claim 10. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 1-3, 5-8, 10-12, 14-17 and 19 under 35 U.S.C. §102(b).

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II. Claims Being Rejected Under 35 U.S.C. § 103**A. Rejections of Claims 4, 13 and 20**

Claims 4, 13 and 20 are rejected under 35 U.S.C. § 103(a) as unpatentable over Yeager. Applicants respectfully traverse the rejection for the following reasons.

Yeager fails to teach or suggest all the elements as recited in claims 1, 10 and 19. Claim 4, 13 and 20, which depend on independent claims 1, 10 and 19, respectively, and therefore incorporate all the patentable features of claims 1, 10 and 19. For at least the same reasons discussed above in connection with of the rejection of claims 1, 10 and 19, Applicants submitted that the Yeager reference fails to disclose all of the elements of claims 4, 13 and 20

Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 4, 13 and 20 under 35 U.S.C. § 103(a).

B. Rejection of Claims 9 and 18

Claims 9 and 18 are rejected under 35 U.S.C. § 103(a) as unpatentable over Yeager in view of Tanebaum, Structured Computer Organization, 2nd Edition, 1984, page 11 ("Tanebaum"). Applicants respectfully traverse the rejection for the following reasons.

Claim 9 and 18 depend on independent claims 1 and 10, respectively. Tanebaum is cited by the Examiner to provide teachings for the subject matter added in claims 9 and 18, which relates to software performing the method recited in claims 1 and 10. Tanebaum, however, does not teach transferring said physical register assignment of said selected physical register from said second structure to a third structure after retirement of said selected instruction. Tanebaum further fails to teach that when the architectural register is assigned as a destination operand for a subsequent instruction, information identifying the selected physical register as available is

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transferred from the third structure to the first structure, as recited in claims 1 and 10. In light of the arguments set forth above, Applicants submit that neither Yeager nor Tanebaum teach or suggest all of the limitations of independent claims 1 and 10. Claim 9 and 18, which depend on independent claims 1 and 10, respectively, are patentable over the cited prior art references. Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 9 and 18 under 35 U.S.C. §103(a).

Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 9 and 18 under 35 U.S.C. §103(a).

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III. Conclusion

In view of the remarks set forth above, Applicants contends that Claims 1-20 presently pending in this application are patentable and in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

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Respectfully submitted,

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